

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Georg Bruederl et al. Art Unit : 2813
Serial No. : 10/561,255 Examiner : Tuan H. Nguyen
Filed : March 31, 2006 Conf. No. : 6533
Title : METHOD FOR THE PRODUCTION OF SEMI-CONDUCTOR CHIPS

Commissioner for Patents
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REQUEST FOR CORRECTED OFFICIAL FILING RECEIPT

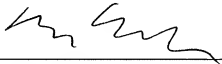
Please correct the Filing Receipt for the above-referenced application to include the correct filing date of the German application priority document. More specifically, the Foreign Applications "GERMANY 10328543.1 06/26/2003" should read --GERMANY 10328543.1. 06/24/2003--. A copy of the cover page of PCT Application No. PCT/DE2004/001329 showing the correct priority date is attached hereto.

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Respectfully submitted,

Date: 12/17/07



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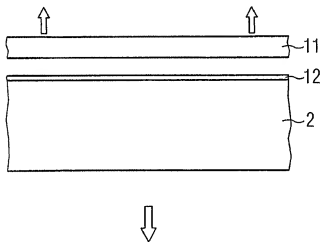
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[Fortsetzung auf der nächsten Seite]

(54) Title: METHOD FOR THE PRODUCTION OF SEMI-CONDUCTOR CHIPS

(54) Bezeichnung: VERFAHREN ZUM HERSTELLEN VON HALBLEITERCHIPS



(57) Abstract: The invention relates to a method for producing a plurality of semi-conductor chips, especially radiation-emitting semi-conductor chips. Said chips comprise, respectively, at least one epitaxially produced functional stack of semi-conductor chips. Said method comprises the following steps: disposing an epitaxial growth substrate wafer (1), which is essentially made of a semi-conductor material which constitutes the same or similar semi-conductor material system in terms of grid parameters as the system on which a semi-conductor layer sequence for the functional semi-conductor stack is based; forming a separation area (4) which is parallel to a main surface (100) of the epitaxial growth substrate wafer (1) in said wafer (1), connecting the epitaxial growth substrate wafer (1) to an auxiliary support wafer (2), separating an opposite section (11) of the epitaxial growth substrate wafer (1) with respect to the

separation area (4), from the auxiliary support wafer (2) along said separation area (4), forming an epitaxial growth surface on the section (12) of the epitaxial growth support surface remaining on the auxiliary support wafer (2) for a subsequent epitaxial growth of the semi-conductor layer sequence; epitaxial growth of the semi-conductor layer sequence (5) on the epitaxial growth surface, depositing a chip substrate wafer on the semi-conductor layer sequence; separating the auxiliary support wafer (2), and dividing the composite semi-conductor layer sequence and chip substrate wafer (7) into individually separated semi-conductor chips.

(57) Zusammenfassung: Verfahren zum Herstellen einer Mehrzahl von Halbleiterchips, insbesondere von strahlungsemitierenden Halbleiterchips, mit jeweils mindestens einem epitaktisch hergestellten funktionellen Halbleiterschichtstapel, das folgende Verfahrensschritte umfasst: - Bereitstellen eines Aufwachssubstratwafers (1), der im Wesentlichen Halbleitermaterial aus einem hinsichtlich Gitterparameter gleichen oder ähnlichen Halbleitermaterialsystem umfasst wie dasjenige, auf dem eine Halbleiterschichtenfolge für die funktionellen Halbleiterschichtstapel basiert, - Ausbilden einer parallel zu einer Hauptfläche (100) des Aufwachssubstratwafers (1) liegende Trennzone (4) im Aufwachssubstratwafer (1), - Verbinden des Aufwachssubstratwafers (1) mit einem Hilfsträgerwafer (2), - Abtrennen eines aus Sicht der Trennzone (4) vom Hilfsträgerwafer (2) abgewandten

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WO 2005/004231 A1



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FILING RECEIPT



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Power of Attorney: The patent practitioners associated with Customer Number 26161.

Domestic Priority data as claimed by applicant

This application is a 371 of PCT/DE04/01329 06/24/2005

Foreign Applications

06/24/2003

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If Required, Foreign Filing License Granted: 06/15/2006

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US10/561,255**

Projected Publication Date: 09/21/2006

Non-Publication Request: No

Early Publication Request: No

Title

Method for the production of semi-conductor chips

Preliminary Class

438

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